**Claims**

1. A parallel processor comprising state element means providing coherent parallel accesses to shared state.

2. A parallel processor as claimed in claim 1, wherein said parallel processor is an array processor.

3. A parallel processor as claimed in claim 2, wherein said array processor is a SIMD processor.

4. A parallel processor as claimed in any of the preceding claims, further comprising means to serialise and/or synchronise multiple accesses/updates to said shared state.

5. A parallel processor as claimed in any of the preceding claims, wherein said state comprises a single item of state.

6. A parallel processor as claimed in any of claims 1 to 4, wherein said state comprises multiple items of state.

7. A parallel processor as claimed in any of claims 1 to 4, wherein said state comprises a single storage location or a data structure in storage.

8. A parallel processor as claimed in claim 1, wherein operations on said state are carried out as a fixed or hardwired set of operations.

9. A parallel processor as claimed in claim 8, further comprising means to supply data to update said state.

10. A parallel processor as claimed in claim 8, further comprising means for sending a command and data to said state, whereby said operations are programmable.

11. A parallel processor as claimed in claim 1, further comprising a plurality of said state element means organised into state cell means, whereby operations on said state can be pipelined.

12. A parallel processor as claimed in claim 11, further comprising a plurality of said state cell means, whereby to allow multiple requests in relation to said state to be handled concurrently.

13. A parallel processor as claimed in claim 12, further comprising input and output interconnect means providing access to and from said state cell means, a bus interface for said input and output interconnect means, said bus interface interfacing with a system bus, and a control unit interconnected with said system bus for controlling accesses to said state.

14. A parallel processor as claimed in any of claims 11 to 13, wherein each said state element means comprises local memory, and each field of a data record is stored in a respective memory of a respective state element means.

15. A parallel processor as claimed in any of the preceding claims, wherein each said state element means comprises a local memory for said state, an arithmetic unit adapted to perform an operation on said state in said local memory, and command and control logic to control said operation.

16. A computer system comprising a parallel processor as claimed in any of the preceding claims.

17. A network processor comprising a parallel processor as claimed in any of the preceding claims.

18. A parallel processor as claimed in any of the preceding claims, implemented on a single silicon chip.